IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

S. NAKAMURA et al

Serial No. 10/086,717 Group Art Unit: 2827

Filed: March 4, 2002 Examiner: D.A. Zarneke

For: A SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

INFORMATION DISCLOSURE STATEMENT (IDS) UNDER § 1.97 AND § 1.98

Commissioner for Patents
Mail Stop DD
Alexandria, VA 22313-1450 June 25, 2003

Sir:

1. This IDS should be considered:

(a) when filed within three months of the filing date of the present application, or within three months of the filing date of the National Stage as set forth in § 1.491 in an international application, or before the mailing date of a first Office Action on the merits, whichever occurs last;

(b) when filed before the mailing date of either a Final Rejection under § 1.113 or a Notice of Allowance under § 1.311, whichever occurs first and when 1(a) does not apply. For this purpose, there is included herein either a certification in section 4 below (included when indicated by a marked box), or a fee of $180.00 (a check in the amount of $180.00 is enclosed, or if not see section 5 below);

(c) when filed prior to the payment of the Issue Fee, when 1(a)-(b) do not apply, and when a certification is included in section 4 below (included when indicated by a marked box); then the Applicant(s) hereby petition(s) and request(s) consideration of this IDS, and provided herewith is a fee of $180.00 (a check in the amount of $180.00 to cover the petition fee, or if not see section 5 below).

2. When 1(a) or (b) do not apply, then it is requested that this IDS be placed in the file.

3. Listing of the information submitted is on the attached Form PTO-1449, which forms a part of this IDS. A copy of each listed document is enclosed when needed (needed for U.S. and foreign patents, publication or portion thereof listed; no copy of a U.S. patent application is needed; a copy of a document is not needed when previously submitted or previously cited by the PTO in a parent application of the present application as set forth under 35 U.S.C. § 120).

4. The undersigned hereby states:

☐☒ (a) that each item of information contained in this IDS was first cited in any communication from a foreign patent office in a counterpart foreign application, as indicated on the copy of the communication submitted herewith, which communication was dated not more than three months prior to the filing of this IDS; or

☐ (b) that no item of information contained in this IDS was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned after making reasonable inquiry, was known to any individual designated in § 1.56(c) more than three months prior to the filing of this IDS.

5. If a fee or additional fee is required, the Commissioner is hereby authorized to charge any fee or additional fee that may be required and credit any excess to Deposit Account No. 50-1417. A duplicate of this sheet is attached.

6. If the PTO determines that part(s) of the required content is inadvertently omitted, then it is requested that the Applicant(s) be given additional time and specific identification of such omission(s) to enable full compliance.

Respectfully submitted,

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Registration No. 32,846
Attorney for Applicants

MATTINGLY, STANGER & MALUR
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Date: June 25, 2003

The Department of Economy

Bureau of the Intellectual Property Right

Notice on Patent Examination and Final Rejection

Acceptors: Hitachi, Ltd.

Hitachi Hokkai Semiconductor, Ltd.

(Agent Lin Chih-kang)

Address: 2-125-7, Nan Ching East Road, Chung Shan District, Taipei

Date of Issue: April 4, 2003

Issuing No.: (92) Intellectual Property 2 (1) 04077

No.09220339270

1. Application No. 091103953

Patent Classification IPC(7) H01L 21/60

2. Title of the Invention:

Semiconductor Device and Its Manufacturing Method

3. Applicants:

Name: Hitachi, Ltd.

Address: Japan

Name: Hitachi Hokkai Semiconductor, Ltd.

Address: Japan

4. Patent Agent:

Name: Lin Chih-kang

Address: 2-125-7, Nan Ching East Road, Chung Shan District, Taipei

5. Filing Date: March 4, 2002

6. Dates of Priority:

1. April 6, 2001; Japan 2001-108603

2. January 22, 2002; Japan 2002-012775

7. Name of the Examiner: Wang Jung-hua

8. Purport of the Decision

Text of judgment: Grant for allowance of the present patent application should be rejected.

Authentic law: Article 20, Item No.2 of the Patent Law

Reasons

(1) "The semiconductor device and its manufacturing method" of the present patent application relate to a multi-chip stack-type package and its object consists in making a thin semiconductor device of multi-layer structure.

(2) A major technical feature of the present patent application consists in an arrangement comprising: a

substrate 3 having a plurality of terminals 3c on a chip supporting surface 3a and having a plurality of soldering balls 11 on a rear surface 3d; a first chip having a major surface 1b and a rear surface 1c, and provided with a plurality of pads 1a and a plurality of semiconductor elements on the major surface 1b; and a second chip having a major surface 2b and a rear surface 2c and provided with a plurality of pads 2a and a plurality of semiconductor elements on the major surface 2b, the second chip having a thinner thickness than that of the first chip; and wires 4 connecting the pads 2a of the second chip with one-chip substrate connector terminals 3c corresponding to the pads. However, Publication No.337036 of July 21, 1998 (see the attached document) discloses a stack-type package having a technical feature similar to the present patent application. That is, as shown clearly in Fig.2 of the citation, the circuit terminals (corresponding to the wires 1a on the present patent application) are directly connected to the first chip by the soldering balls (corresponding to the soldering balls 11 of the present patent application) to be arranged on a base member, and the second chip is placed on the first chip and the circuit terminals are joined on the base member by the wire bonding (corresponding to the wires

4 of the present patent application). In addition, the technical feature in which the second chip is made thinner than the first chip could be easily realized by those skilled in the art of semiconductor package in reference to an understanding of the technical feature of the citation in order to make a thin multi-layer structure.

(3) With the foregoing argument, the present patent application is based on the prior art or knowledge and could easily be realized by those skilled in the art.

As a conclusion, the present patent application does not coincide with the legal patent requirement and shall be decided as described in the text of judgment under the provision of Article 20, Item No.2 of the Patent Law.

This decision has been executed mainly by a section in charge of authorization under the provision in which each of the organizations should bear the responsibility.

If applicant has a certain complaint against this decision, the applicant can request to file a re-examination with this bureau within 30 days counted from a next day of arrival of this notice by submitting two copies of one set of Reasons for Re-Examination together with new Taiwan 6,000 dollars (if pages of the specification and the drawings exceed 50 pages or more,

new Taiwan 500 dollars shall be added for every 50 pages, and in turn if pages of the specification and the drawings are lower than 50 pages, they shall be counted as 50 pages).

FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. H 1034	SERIAL NO. 10/086,717

LIST OF DOCUMENTS CITED BY APPLICANT
(Use several sheets if necessary)

APPLICANT	
S. NAKAMURA et al	
FILING DATE	GROUP
March 4, 2002	2827

U.S. PATENT DOCUMENTS

* EXAMINER INITIAL		DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE (If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

		DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATIO YES	TRANSLATIO NO
	AL	337036	7-21-98	Taiwan			☐	☐
	AM						☐	☐
	AN						☐	☐
	AO						☐	☐
	AP						☐	☐

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, etc.)*

	AR		
	AS		
	AT		

EXAMINER DATE CONSIDERED

EXAMINER